REMARKS/ARGUMENTS

Figure 5 has been amended such that its notations be consistent as described in the detailed description of the application.

Claim rejections
35 USC § 112

In section 2 of the above referenced Office Action, Claims 1-20 were rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. The Applicant respectfully traverses the rejection.

It is respectfully asserted that there is support in the specification for *"detecting an I/O read instruction followed by a conditional jump instruction."* The example to follow is to illustrate that there is support in the specification and not intended to limit the scope of Claims 1-20.

35 USC 112, paragraph 6 states:

"An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof."

Independent Claim 1 recites a *"virtual microcontroller having means for detecting an I/O read instruction followed by a conditional jump instruction."* As such, the specified element is expressed as means for performing a specified

function, detecting an I/O read instruction followed by a conditional jump instruction. Consequently, no recital of the structure in support of the specified function is needed in the claim. Furthermore, the recited element of independent Claim 1 shall be construed to cover the corresponding structure described in the specification and equivalents thereof.

The Examiner is respectfully directed to page 27 line 5 to page 28 line 8 of the specification, reciting that virtual microcontroller computes the target jump location as the I/O data is being received and that before the actual jump the virtual microcontroller evaluates the conditional jump and either uses the pre-computed jump information if the condition is true or that it simply increments the program counter otherwise. It is understood by those skilled in the art that such detection can be purely hardware based (e.g., combinational logic), software based (e.g., sequential logic), or some combination of the two. Therefore, the language of the limitation, detecting an I/O read instruction followed by a conditional jump instruction, should be construed as described in the specification or equivalent thereof. As such, independent Claim 1 is fully supported by the specification and complies with the written description requirement. Accordingly, the Applicant respectfully requests the withdrawal of the rejection for independent Claim 1, under 35 USC 112, first paragraph.

Claims 2-5 depend from independent Claim 1. Accordingly, Claims 2-5 comply with 35 USC 112, first paragraph at least for the same reasons that independent Claim 1 complies with 35 USC 112, first paragraph. As such, withdrawal of the rejection for Claims 2-5, under 35 USC 112, first paragraph is earnestly solicited.

Independent Claims 6 and 14 have been amended to particularly point out that the specific instructions that are detected are an I/O read instruction followed immediately by a conditional jump instruction. The Examiner is respectfully directed to page 27 line 5-12 of the specification. As such, withdrawal of the rejection for Claims 6 and 14, under 35 USC 112, first paragraph is earnestly solicited.

Claims 7-13 and 15-20 depend from independent Claims 6 and 14 respectively. Accordingly, Claims 7-13 and 15-20 comply with 35 USC 112, first paragraph at least for the same reasons that independent Claims 6 and 14 comply with 35 USC 112, first paragraph. As such, withdrawal of the rejection for Claims 7-13 and 15-20, under 35 USC 112, first paragraph is earnestly solicited.

In section 3 of the above referenced Office Action, Claims 1-20 were rejected under 35 USC 112, first paragraph, as allegedly failing to comply with the enablement requirement. The Applicant respectfully traverses the rejection.

With regard to the enablement requirement of independent Claims 1, 6 and 14 referring to *"detecting an I/O read instruction followed by a conditional jump instruction,"* the Examiner is respectfully directed to page 27 line 5 to page 28 line 8 of the specification, reciting that virtual microcontroller computes the target jump location as the I/O data is being received and that before the actual jump the virtual microcontroller evaluates the conditional jump and either uses the pre-computed jump information if the condition is true or that it simply increments the program counter otherwise. It is understood by those skilled in the art that such detection can be purely hardware based (e.g., combinational logic), software based (e.g., sequential logic), or some combination of the two. Accordingly, independent Claims 1, 6 and 14 meet the enablement requirement of 35 USC 112, first paragraph. As such, withdrawal of the rejection for Claims 1, 6 and 14 under 35 USC 112, first paragraph is earnestly solicited.

Claims 2-4, 7-13 and 15-20 depend from independent Claims 1, 6 and 14 respectively. Accordingly, Claims 2-4, 7-13 and 15-20 comply with 35 USC 112, first paragraph at least for the same reasons that independent Claims 1, 6 and 14

comply with 35 USC 112, first paragraph. As such, withdrawal of the rejection for Claims 2-4, 7-13 and 15-20, under 35 USC 112, first paragraph is earnestly solicited.

Claim rejections
35 USC § 103

In section 4 of the above referenced Office Action, Claims 1-20 were rejected under 35 USC 103(a) as being allegedly unpatentable over Profit, Jr U.S. Pat. No. 5,911,059 (hereinafter, Profit) in view of Barnett U.S. Pat. No. 6,173,419 (hereinafter, Barnett).

Newly amended independent Claim 1 recite *"a virtual microcontroller ... executing instructions in lock-step with the microcontroller by executing the same instructions using the same clocking signals and ... computing a conditional jump address prior to receipt of I/O read data from the microcontroller to remain in lockstep execution with said microcontroller."* Accordingly, the virtual microcontroller and the microcontroller execute instructions in lock-step by executing the same instruction using the same clock signals. Furthermore, the virtual microcontroller cannot compute the jump address in sufficient time to remain in lockstep execution with the real microcontroller, thus microcontroller pre-calculates the jump address. Moreover, executing the same instruction using the same clock signals and pre-calculating the jump address to remain in lock-

step execution necessarily suggest that the microcontroller and the virtual microcontroller do not get out of synch.

Profit discloses that communications interface performs two primary functions, one of which is resynchronization of the target program and target circuitry on a periodic basis. (See Profit, col. 7, lines 31-52). As such, Profit suggests that the target program and target circuitry go out of synch, hence requiring resynchronization using a communication interface.

Newly amended independent Claim 1 distinguishes over Profit by reciting "a virtual microcontroller ... executing instructions in lock-step with the microcontroller by executing the same instructions using the same clocking signals and ... computing a conditional jump address prior to receipt of I/O read data from the microcontroller to remain in lockstep execution with said microcontroller." In contrast, Profit uses additional circuitry (e.g., communication interface) in order to resynchronize the target program and the target circuitry whereas in independent Claim 1 not only no additional circuitry is used to execute instruction in lock-step (e.g., by executing same instructions using the same clocking signal and by pre-calculating the jump address) but the microcontroller and the virtual microcontroller do not go out of synch either. As such, Profit does not disclose executing instructions in lock-step by executing the same instructions using the same clocking signals nor Profit suggest pre-calculating jump instruction to execute instructions in lock-step.

The above referenced Office Action admits that Profit does not teach that the hardware simulator be implemented in an FPGA. The Examiner relies on Barnett to overcome this defect. The Applicant respectfully disagrees that Barnett remedies this defect. Assuming arguendo that Barnett remedies this defect, the combination of Profit and Barnett still does not teach the limitations of independent Claim 1 because neither Profit nor Barnett disclose executing instructions in lock-step by executing the same instructions using the same clocking signals or suggest pre-calculating jump instruction to execute instructions in lock-step.

Accordingly, the combination of Profit and Barnett does not render newly amended independent Claim 1 obvious, under 35 USC 103(a). As such, allowance of independent Claim 1 is earnestly solicited.

Newly amended independent Claims 6 and 14 are similar in scope to that of independent Claim 1. Accordingly, the combination of Profit and Barnett does not render independent Claims 6 and 14 obvious, under 35 USC 103(a) at least for the same reasons that independent Claim 1 is not rendered obvious. As such, allowance of independent Claims 6 and 14 is earnestly solicited.

Claims 2-5, 7-13 and 15-20 depend from independent Claims 1, 6 and 14 respectively and are not rendered obvious in view of the combination of Profit

and Barnett, under 35 USC 103(a), at least for the same reasons that independent Claims 1, 6 and 14 are not rendered obvious. As such, allowance of Claims 2-5, 7-13 and 15-20 is earnestly solicited.

For the above reasons, the Applicant requests reconsideration and withdrawal of these rejections under 35 U.S.C. 112 and 35 U.S.C. §103.

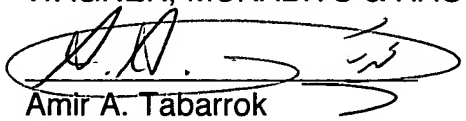
CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-20 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-20 overcome the rejections of record and, therefore, allowance of Claims 1-20 is earnestly solicited.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,
WAGNER, MURABITO & HAO LLP

Dated: Jan 17, 2006



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